Hardware Implementation of Three Level NPC Inverter Using dSPACE DS1104 Controller Interface

Umashankar S[1], Ratika Singh Rawat[2], Priyanka Rana[2], Nakul Thombre[2]

[1]Professor, [2] PG Student
School of Electrical Engineering
VIT University, Vellore
Tamilnadu, India

ABSTRACT

This paper presents the close loop control modeling and prototype implementation of conventional three level Neutral Point Clamped Multilevel Inverter (NPC-MLI) using dSPACE DS1104 controller platform. This paper focuses on hardware implementation of three level NPC inverter using dSPACE controller and balancing the Neutral Point Potential (NPP), hereby reducing the output voltage distortion. The real time controller platform can link simulation model developed in MATLAB (R2012a) to the hardware prototype. The dSPACE kit generates the SPWM logic pulses to trigger inverter switches. Designing of close loop control strategy results in regulation of dc-link capacitor voltages and significant reduction in the voltage distortion at the neutral point allowing reduction of the required dc-bus capacitance. The flexibility of dSPACE allows development of simulink logic for pulse generation.

1. INTRODUCTION

The Three-Level Neutral Point Clamped Multilevel Inverter is now becoming popular technology for medium voltage , high power applications such as variable speed drives, power compensation, rolling mills and renewable energy applications [1-2]. The reason behind the increasing popularity of DCMLI is the better quality of output voltage which involves the reduced harmonic distortion, lesser voltage stress across switches and nearly sinusoidal output waveform generation [3]. A neutral point clamped inverter is also called Diode clamped (DC) is the most widely used inverter among all multilevel inverters [4]. One of the inherent problem in the NPC MLI is deviation of neutral point potential due to non uniform charge distribution across dc-bus capacitor, load unbalancing and dissimilarity in dc-bus capacitors provided from the manufacturer [5-6]. Occurrence of unbalancing in dc- bus voltage the neutral point potential (NPP) deviates from its reference value which is zero. As a result it simultaneously introduces harmonics in the output voltage. To maintain the NPP and reduce the total harmonic distortion (THD) in output voltage, the potential across each capacitor of the dc-bus must be maintained to the half of the total supply voltage. To achieve the fore-mentioned objective a close loop control strategy with dSPACE which is less sensitive to environmental temperature is implemented.

2. THREE- LEVEL NEUTRAL POINT CLAMPED INVERTER

The simplified circuit diagram of three-level NPC inverter is shown in fig.1. The inverter leg ‘a’ contains four switches Sa1 to Sa4 and four anti parallel diodes. Practically, either IGBT or GCT can be preferred as switching device [7]. The input dc side of inverter, dc bus capacitor is split into two, creating a neutral point Z. The diodes, D_{a1} and D_{a2} connected to the neutral point Z, are called the clamping diodes which clamps the inverter terminal voltage to NPP. When switches Sa2 and Sa3 are turned on, the inverter output terminal ‘a’ is connected to the NP through one of the clamping diodes. The potential across each of the dc capacitors is V1=V2, which is normally equal to half of total applied dc voltage V_d. The capacitors C_1 and C_2 can be charged or discharged by neutral current, generating a NPP deviation .The switching states of conventional three level NPC is shown in Table.I

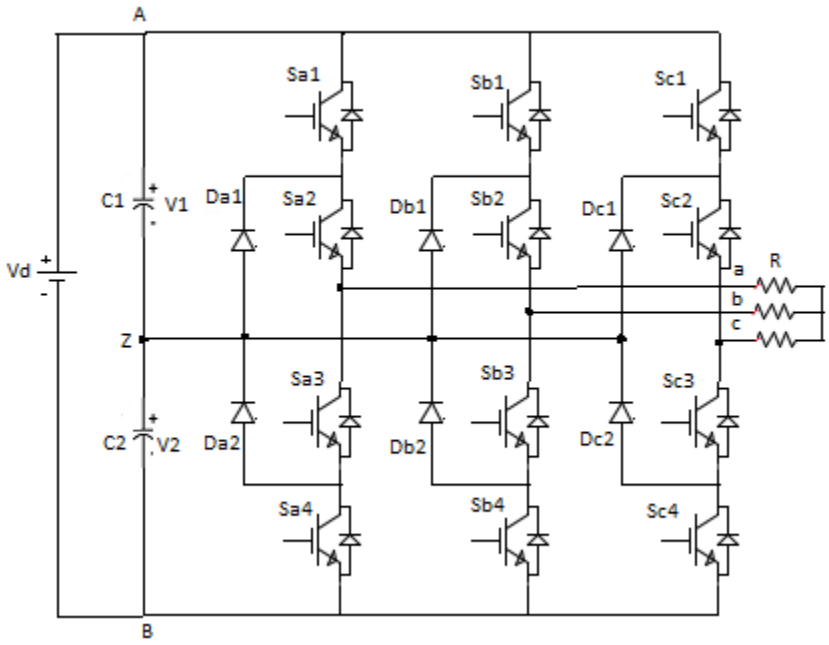

Fig. 1 Structure of DCMLI

Table I. Switching States Of Three Level NPC Inverter

Sr no.	Switching State	Device Switching Status (Phase A)				Inverter terminal Voltage
		S1	S2	S3	S4	V_{AZ}
1)	+	ON	ON	OFF	OFF	+Vd/2
2)	0	OFF	ON	ON	OFF	0
3)	-	OFF	OFF	ON	ON	-Vd/2

2.1 DESIGN OF CLOSED LOOP CONTROL FOR THREE LEVEL NPC INVERTER

Closed loop control in three level diode clamped inverter is done by using Dc-link voltage and Load voltage control loop.This DC level injection control strategy for capacitor balancing holds the determination of the magnitude of variable offset voltage based on the average value, total harmonic distortions, peak-to-peak amplitude and third harmonic content in NPP. The complete Simulink model of DC level injection control strategy is shown in Fig.2.

The load voltage Vabc is sensed at the 3-phase resistive load which is taken as feedback element. The load voltage Vabc is converted into per unit by using abc to per unit conversion Vabc (pu). These per unit voltages are fed to three phase to two phase conversion ,at the output of conversion block Vdqo are compared with reference values of dqo voltages. It generates a voltage error which is fed to PI controller which regulates the error and generates V*dqo.

After the conversion the three phase waveform V*abc is produced which is taken as the reference signal given as input to the 3-level PWM generator. The 3-level PWM generator consists of two high frequency carrier signals of 2 KHz which is compared with the reference signal to produce the gate pulses for the switches of the inverter to produce the three level output waveform. In load voltage control loop method PI controller is used which is used to control the load voltage only it does not able to control the neutral point potential. The difference between two dc-link voltages (i.e., Vnp = V1 − V2) is calculated by DC voltage loop, and the error is fed to PI controller. Then at its output, variable offset voltage (Voff) is generated. A continuous variable offset Voff voltage regulates the midpoint potential of the dc-bus and rectifies any existing imbalance in the dc- link voltage. This offset voltage Voff is added with the three phase sinusoidal reference signal Vabc to generate a new reference signal. The new reference signal is given as input to the 3-level PWM generator. The reference signal is compared with the carrier signal and produces the gate pulses for the switches of the inverter to produce the three level output waveform. In dc-link voltage control loop the neutral point potential is minimized upto some extent by adding the offset voltage to reference signal.

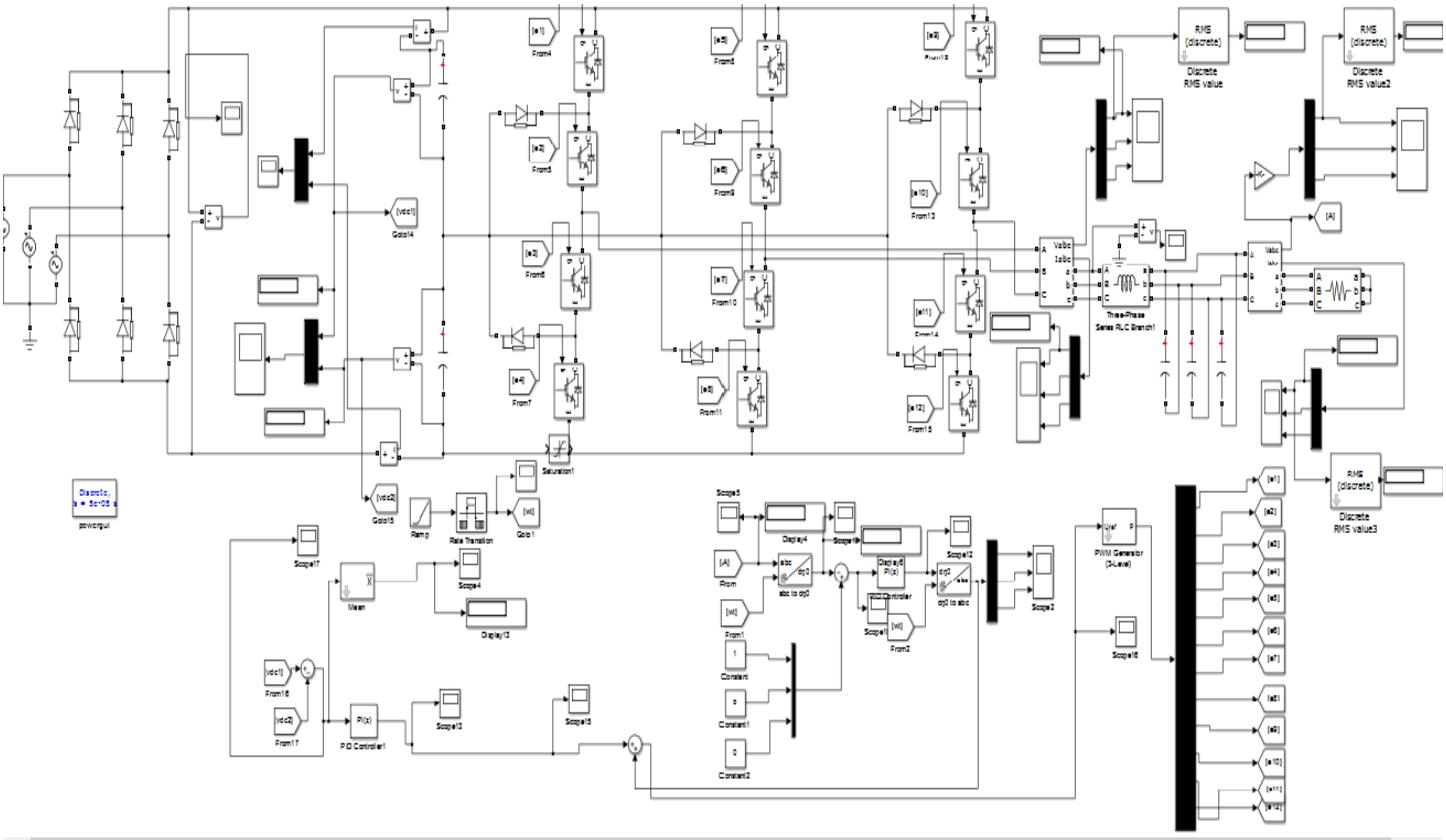

Fig 2. Simulink model of DC level injection method for capacitor balancing

2.2 HARDWARE IMPLEMENTATION OF THREE LEVEL NPC INVERTER USING DSPACE

The dSPACE control platform simplifies the programming task using library block set and interfacing of control algorithm to run on processor and on-chip peripherals. In the hardware part open loop simulation has been presented with real time simulation implementation. This is achieved by using digital signal processor controller. dSPACE and MATLAB interface is being made to achieve pulse generation.DS 1104 is used for PWM generation by SPWM technique. The important blocks or modules while implementation is described in Fig.3.The specification of each component used in hardware setup is shown in Table II.

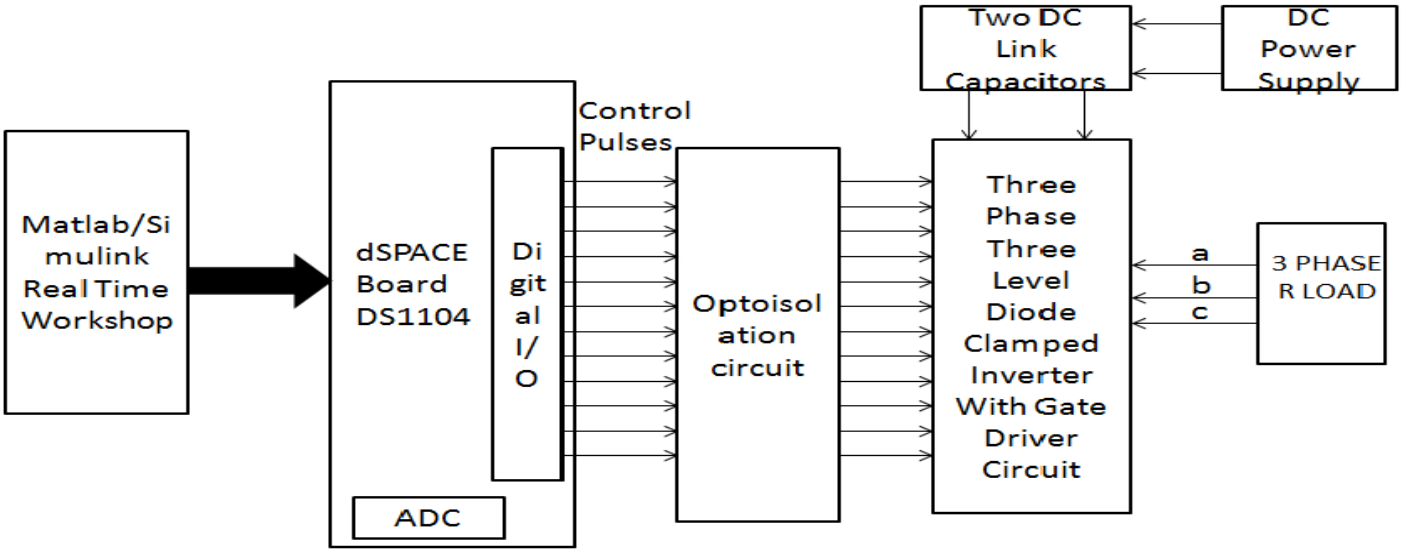

Fig. 3 Complete Block Diagram of dSPACE-DS1104 based Three Phase Three Level Diode Clamped Inverter Experimental Setup

An optoisolated interface board is used to isolate the entire DSP master bit I/O in RTI Library block. The interface between the MATLAB/Simulink and dSPACE DS1104 allows the control algorithm to be run on the processor which is a 64-b floating point MPC8240 processor with a PPC603e core and on-chip peripherals. The master bit I/O is used to generate the required 12 gate pulses. The hardware setup for the experimentation of three level diode clamped inverter is shown in Fig.5 where the component and their names are specified

Table II. Component Table for Hardware Setup

S.No	Name of the Component	Specification
1.	DC link Voltage	24 V
2.	DC link Capacitor	2200 µF
3.	MOSFET	IRF 840
4.	Diode	BY 329
5.	R Load	1KOhm
6.	Opto-isolator	TLP 250

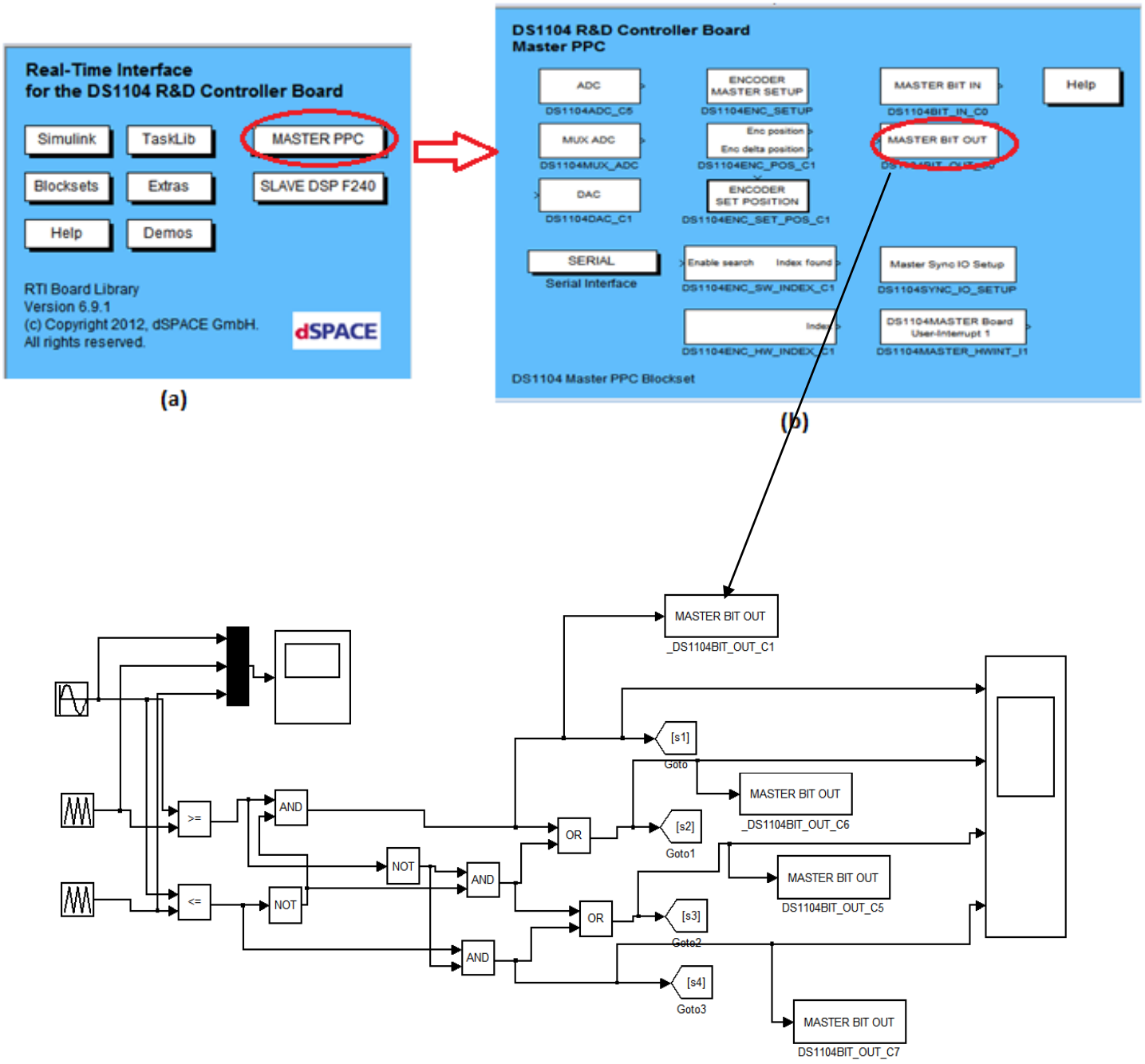

Fig. 4 (a) Real-Time Interface (RTI) DS1104 Library block (b) RTI library Master PPC block (c) Simulink model for Pulse Generation in Diode Clamped Inverter (Phase A)

The Fig.4 (a) shows Real Time Interface (RTI) for DS1104 R & D controller board opened in MATLAB.From this RTI Board library, Master PPC is selected and opened .From the window opened shown in Fig.4(b) Master Bit out block is used in the pulse generation circuitry for the three level NPC inverter.The Fig.4(c) shows the simulink model for the pulse generation of three level NPC inverter for Phase A.

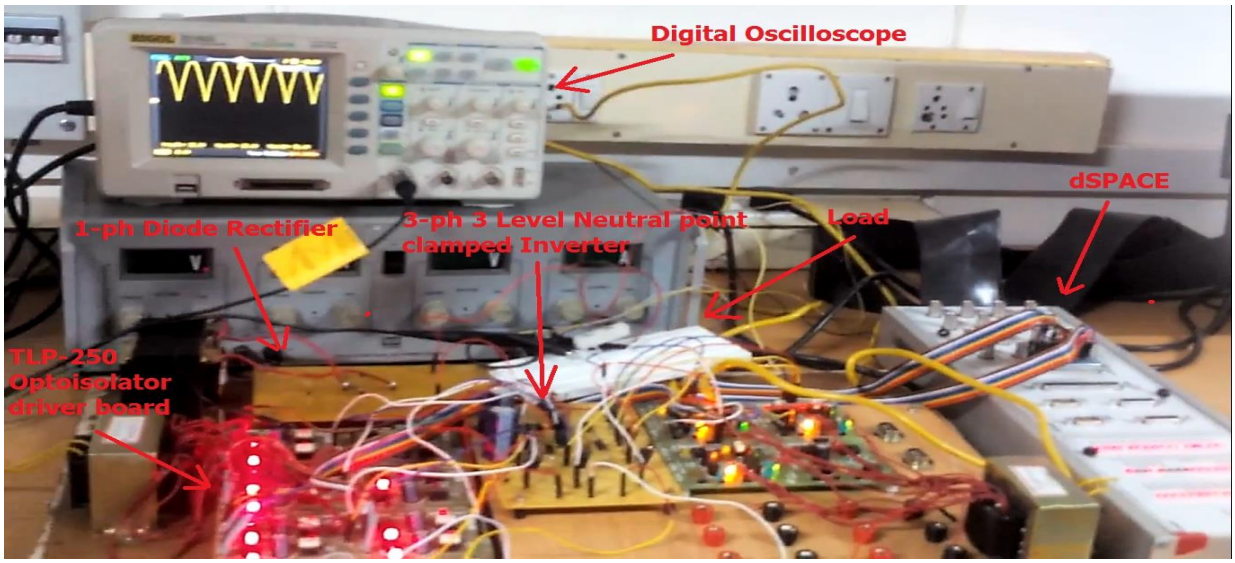

Fig.5 Hardware Experimentation of Three Level Diode Clamped Inverter

The following advantages of using dSPACE are:

- Provides a platform for Real Time Interface (RTI) applications which replaces the requirement of validation of physical system.
- The reconfigurability of dSPACE allows development of simulink logic for pulse generation and directly dumped on dSPACE kit.
- Takes less time to implement different control algorithms.
- The SPWM pulses from Digital I/O pins are obtained with increased efficiency and given to isolation circuitry.

2.3 SIMULATION RESULTS:

Here in Fig.6 capacitor voltage is balancing at t= 0.08 sec.

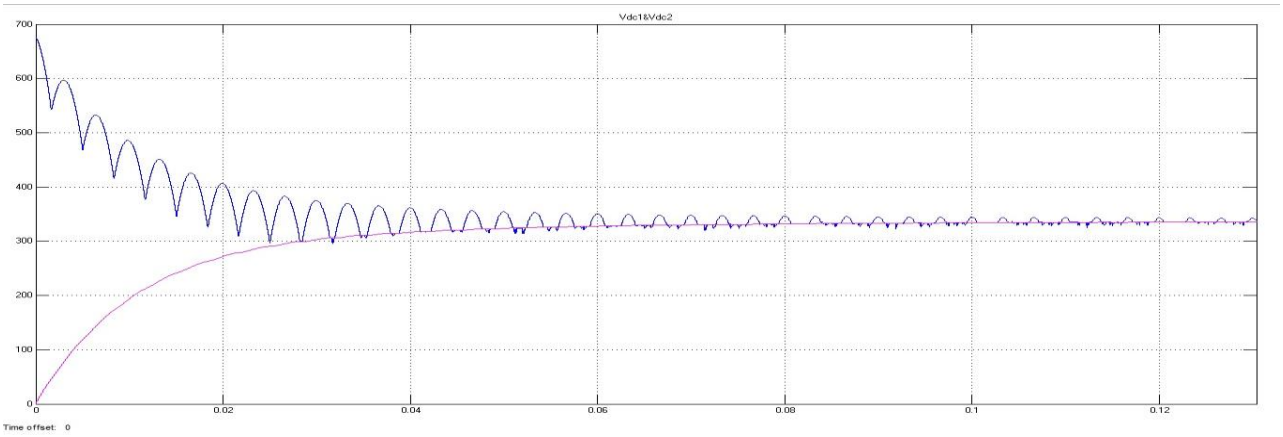

Fig.6 Simulated Capacitor voltages waveforms [Vdc1(blue), Vdc2(red)] after applying close loop control strategy

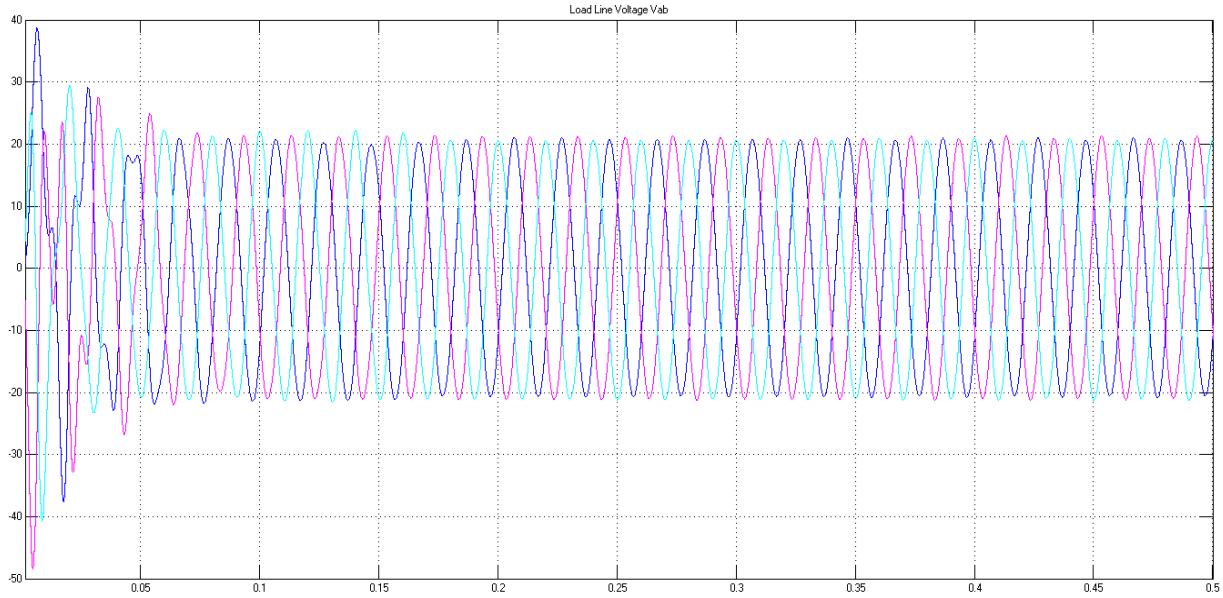

Fig.7 Simulated output current Waveform after applying close loop control strategy

The Fig.7 shows output current after applying 2nd control strategy. After t= 0.25sec, output current is balanced.

2.4 HARDWARE RESULTS:

Following Fig.8 shows the pulses given to the one leg of the 3 level NPC inverter using dSPACE:

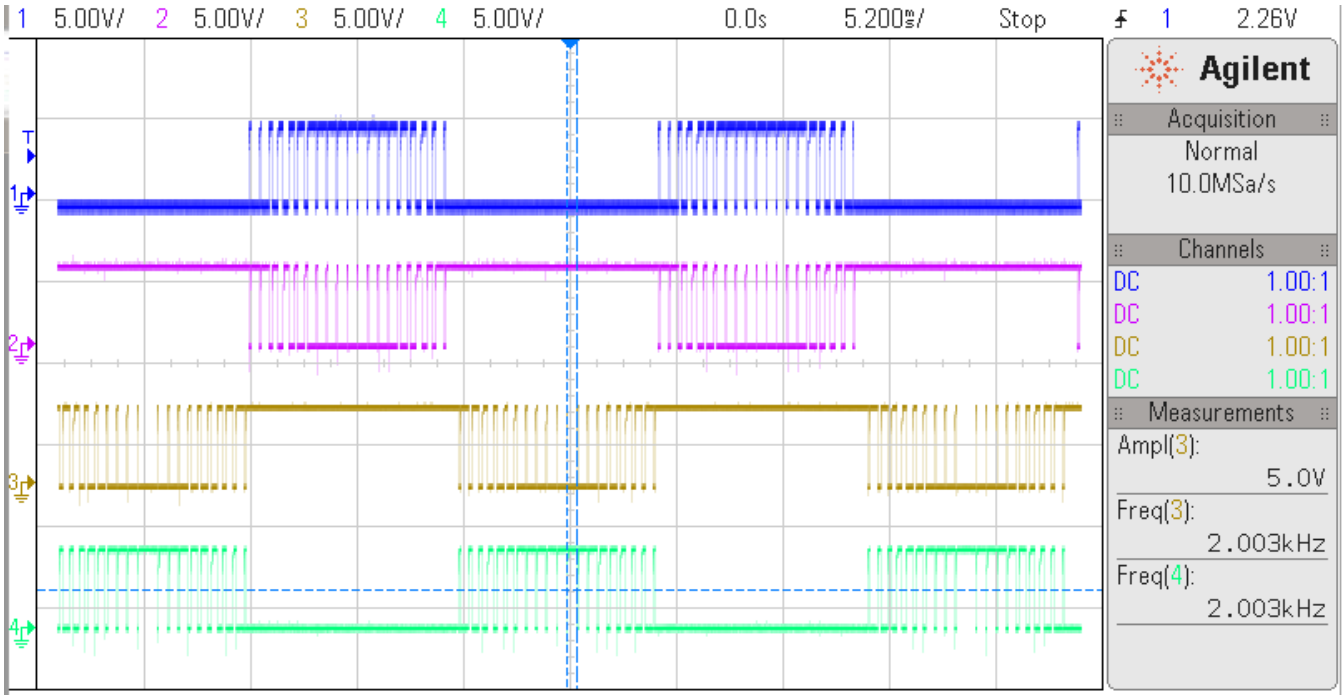

Fig.8 Switching Pulses to generate the Output voltage of Phase "A"

Following Fig.9 shows capacitor voltage waveform (v1):

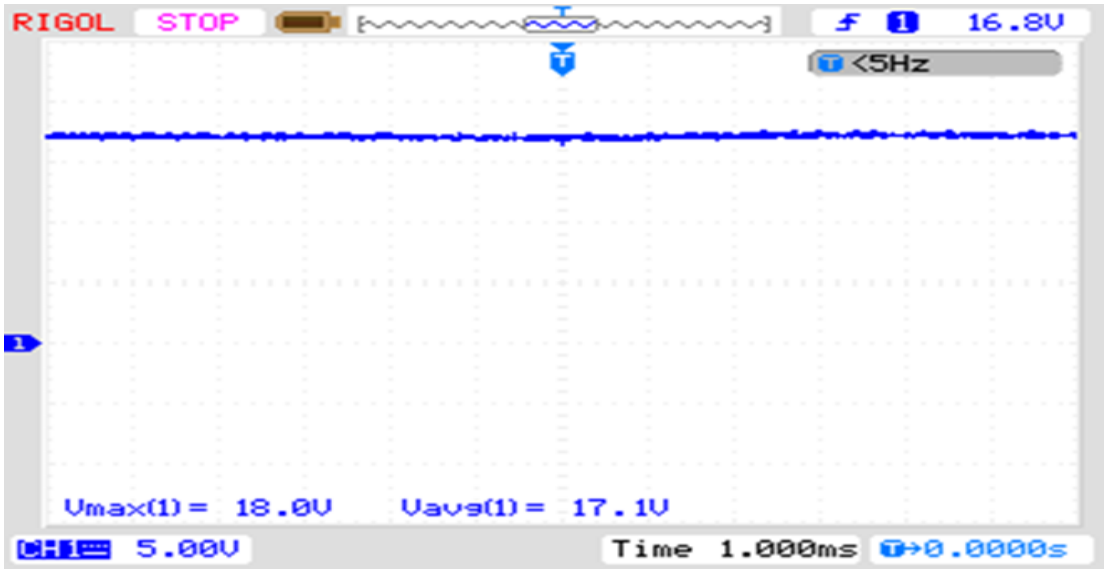

Fig.9 Capacitor voltage waveform (V1)

Following Fig. 10 shows capacitor voltage waveform (v2) across the lower capacitor:

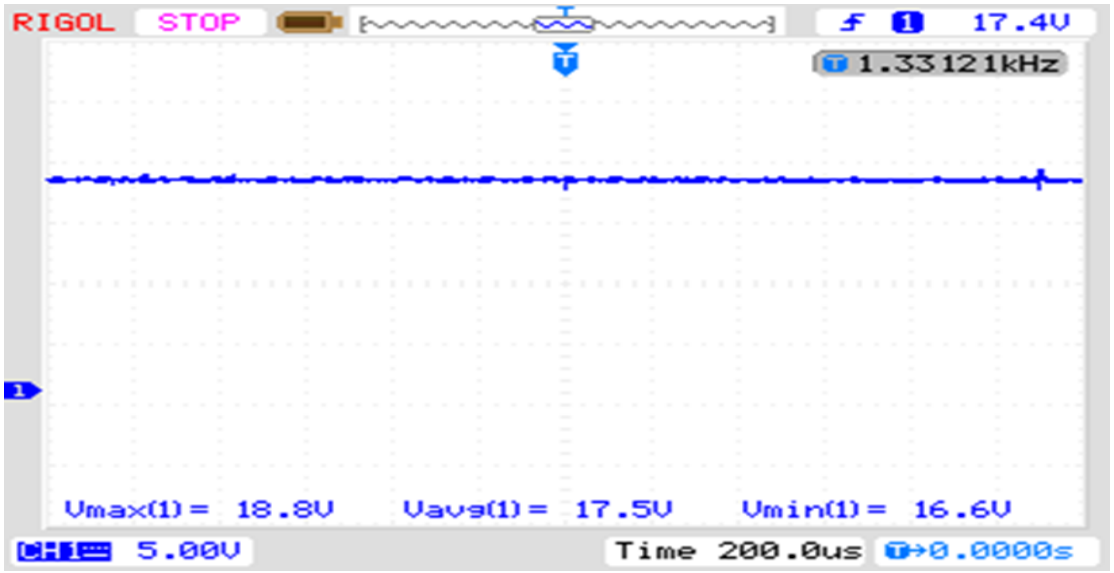

Fig.10 Capacitor voltage waveform (V2)

The following Fig. 11 shows 3 level output voltage of NPC inverter

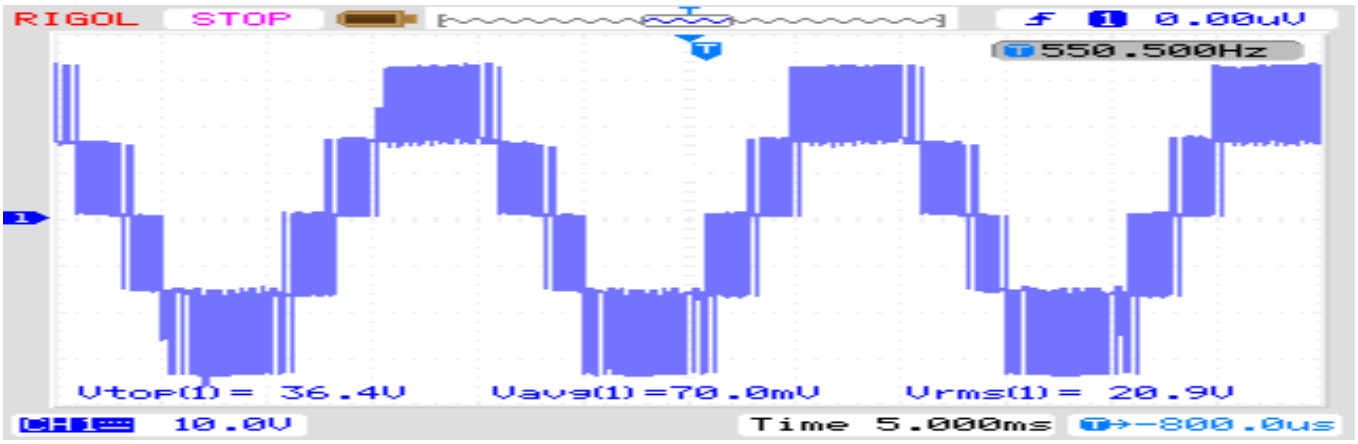

Fig. 11 Output waveform of Inverter Line-Line Voltage

3. CONCLUSION

In this paper, the prototype of 3 level three phase NPC inverter is implemented using dSPACE.Here only open loop implementation is shown for 3 level NPC inverter and from the waveforms in Fig.9 and Fig .10 shows that unbalancing of voltage across each capacitor. Pulse generation algorithm to trigger inverter switches is implemented on hardware with the help of Real Time Interface (RTI) between the Matlab /Simulink and dSPACE DS 1104.In another section,the closed loop simulation of DC level injection method for capacitor balancing is based on adding a continuous variable offset voltage which regulates the midpoint potential of the dc bus. Also, the Neutral point potential is balanced using the same control strategy and verified using MATLAB/Simulink.

4. ACKNOWLEDGMENT

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5. REFERENCES

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